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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/010,905 | 10/18/2001 | Olli Makipaa | 602.355USW1 | 6132 |

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SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

| EXAMINER | |
|---|---|
| CHU, GABRIEL L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2114 | |

DATE MAILED: 06/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/010,905 | MAKIPAA ET AL. | |
| | Examiner | Art Unit | |
| | Gabriel L. Chu | 2114 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *18 October 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Objections*

1. Claims 1, 4, 6, and 7 are objected to because of the following informalities:

Referring to claim 1, "the first plug-in unit" has no antecedent basis. It is understood to refer to "a first plug-in unit of the at least two plug-in units".

Further referring to claim 1, "the bus address is transferred in conjunction with a reboot from the first register" is unclear. It is instead understood to refer to "the bus address is transferred, in conjunction with a reboot, from the first register".

Referring to claims 4 and 6, "transferring the bus address in conjunction with a reboot from the first register" is unclear. It is understood to refer to "transferring the bus address, in conjunction with a reboot, from the first register".

Further referring to claim 6, "means for connected" is understood to refer to "means for connecting".

Further referring to claim 6, "the bus address" has no antecedent basis. It is understood to refer to "a bus address".

Referring to claims 6 and 7, "the second register" has no antecedent basis. In claim 6, "a subscriber" is understood to refer to "a second register".

Further referring to claim 7, "the operation and maintenance facility" has no antecedent basis. It is understood to refer to "an operation and maintenance facility".

Appropriate correction is required.

### *Specification*

2. The disclosure is objected to because of the following informalities:

Referring to line 15 of page 3 of the specification, "bust" is understood to refer to "bus".

Appropriate correction is required.

3. Applicant is further advised to proofread the specification for any typographical and grammatical errors that remain.

***Claim Rejections - 35 USC § 102***

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claim 6 ~~is~~ -1 are rejected under 35 U.S.C. 102(b) as being anticipated by US 6032271 to Goodrum et al. Referring to claim 6, Goodrum et al. disclose an interface circuit, comprising: means for connecting a first bus to a plug-in unit (From the abstract, "The devices are coupled to a bus." Further, from figure 2, 36.); a first register; and a second register, wherein the interface circuit comprises: means for transferring a bus address into the first register (From line 44 of column 88, "Referring to FIG. 39, the BIOS isolation handler first logs 408 to the fail status information portion of the NVRAM the bus history and bus state vector information stored in the history and vector FIFOs in the bus monitor 127."); and means for transferring the bus address, in conjunction with a reboot, from the first register into the second register (From line 11 of column 88,

"Referring to FIG. 38, a BIOS ASR handler is invoked in response to an ASR reboot condition. The ASR handler first checks 444 to determine if an isolation-in-progress event variable (EV) contains active information indicating that the isolation process was in progress prior to the ASR time-out event. The isolation-in-progress EV is stored in non-volatile memory (NVRAM) 70 and includes header information which is set active to indicate that the isolation process has started. The isolation-in-progress EV is also updated with the current state of the isolation process, including the slots which have been checked, the slots which are defective, and the slots which have been enabled.").

Referring to claim 7, Goodrum et al. disclose the interface circuit comprises means for sending the bus address from the second register to an operation and maintenance facility (From line 23 of column 88, "If the isolation process was in progress, the BIOS ASR handler re-enables 448 all slots except the ones that were enabled immediately prior to the ASR event, which is determined from the isolation-in-progress EV.").

***Claim Rejections - 35 USC § 103***

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 2, and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6032271 to Goodrum et al. in further view of US 5878237

to Olarig. Referring to claim 1, Goodrum et al. disclose a method for identifying a defective plug-in unit in a system comprising a first bus (Figure 3, 24.); an interface circuit provided with a first register and a second register (Figure 1, 70.); at least two plug-in units connected via interface circuits to the first bus (From figure 1, 36. Further from line 61 of column 6, "It also includes logic for reading the engagement status of the levers 802, and the status of the cards 807 in each slot 36."); a second bus connected to at least one plug-in unit (From figure 1, 17, via 15 and 26.); and an operation and maintenance facility connected to the second bus (From figure 1, 72 and 23. Further from line 11 of column 88, "Referring to FIG. 38, a BIOS ASR handler is invoked in response to an ASR reboot condition."); wherein a bus address is transferred into the first register (From line 44 of column 88, "Referring to FIG. 39, the BIOS isolation handler first logs 408 to the fail status information portion of the NVRAM the bus history and bus state vector information stored in the history and vector FIFOs in the bus monitor 127."); and the bus address is transferred, in conjunction with a reboot, from the first register into the second register (From line 11 of column 88, "Referring to FIG. 38, a BIOS ASR handler is invoked in response to an ASR reboot condition. The ASR handler first checks 444 to determine if an isolation-in-progress event variable (EV) contains active information indicating that the isolation process was in progress prior to the ASR time-out event. The isolation-in-progress EV is stored in non-volatile memory (NVRAM) 70 and includes header information which is set active to indicate that the isolation process has started. The isolation-in-progress EV is also updated with the current state of the

isolation process, including the slots which have been checked, the slots which are defective, and the slots which have been enabled."). Although Goodrum et al. do not specifically disclose that the first plug-in unit addresses the second plug-in unit with the bus address, device-to-device transactions are well known in the art. An example of this is shown by Olarig from line 31 of column 9, "In the present invention, PCI device to PCI device transactions are also contemplated herein. When a PCI device on a physical PCI bus addresses another PCI device's memory or I/O addresses on the same physical PCI bus or on another physical PCI bus, this is referred to hereinafter as "peer-to-peer" PCI bus transactions. It is contemplated in the present invention that peer-to-peer transactions may be enabled or disabled by setting a control register bit in the core logic. The present invention may broadcast the peer-to-peer transaction address onto the physical PCI buses so that the intended PCI target may respond. Once the target PCI device responds, the peer-to-peer transaction is completed. There is no host bus or memory bus activity required for peer-to-peer PCI bus transactions. Concurrent transaction activity may occur, however, on other physical PCI buses between the memory bus and/or host bus as more fully described hereinafter. This is especially useful when using intelligent, distributed input-output ("I/O") processing as more fully defined in the "Intelligent Input/Output" ("I.sub.2 O") specification, entitled "Intelligent I/O (I.sub.2 O) Architecture Specification," Draft Revision 1.5, dated March 1997; the disclosure of which is incorporated by reference hereinabove." A person of ordinary skill in the art at the time of the invention would have been motivated to perform a device-to-device transfer

because there is a need to communicate between peer devices.

Referring to claim 2, Goodrum et al. in view of Olarig disclose the bus address is read from the second register by means of the operation and maintenance facility (From line 23 of column 88 of Goodrum et al., "If the isolation process was in progress, the BIOS ASR handler re-enables 448 all slots except the ones that were enabled immediately prior to the ASR event, which is determined from the isolation-in-progress EV.").

Referring to claim 4, Goodrum et al. disclose a system for identifying a defective plug-in unit, said system comprising: a first bus (Figure 3, 24.); an interface circuit provided with a first register and a second register (Figure 1, 70.); at least two plug-in units connected via interface circuits to the first bus (From figure 1, 36. Further from line 61 of column 6, "It also includes logic for reading the engagement status of the levers 802, and the status of the cards 807 in each slot 36."), a second bus connected to at least one plug-in unit (From figure 1, 17, via 15 and 26.); and an operation and maintenance facility connected to the second bus bus (From figure 1, 72 and 23. Further from line 11 of column 88, "Referring to FIG. 38, a BIOS ASR handler is invoked in response to an ASR reboot condition."), wherein the system comprises: means for transferring the bus address into the first register (From line 44 of column 88, "Referring to FIG. 39, the BIOS isolation handler first logs 408 to the fail status information portion of the NVRAM the bus history and bus state vector information stored in the history and vector FIFOs in the bus monitor 127."); means for transferring the bus address, in conjunction with a reboot, from the first register into the second

register (From line 11 of column 88, "Referring to FIG. 38, a BIOS ASR handler is invoked in response to an ASR reboot condition. The ASR handler first checks 444 to determine if an isolation-in-progress event variable (EV) contains active information indicating that the isolation process was in progress prior to the ASR time-out event. The isolation-in-progress EV is stored in non-volatile memory (NVRAM) 70 and includes header information which is set active to indicate that the isolation process has started. The isolation-in-progress EV is also updated with the current state of the isolation process, including the slots which have been checked, the slots which are defective, and the slots which have been enabled."); and means for reading the bus address from the second register by using the operation and maintenance facility (From line 23 of column 88 of Goodrum et al., "If the isolation process was in progress, the BIOS ASR handler re-enables 448 all slots except the ones that were enabled immediately prior to the ASR event, which is determined from the isolation-in-progress EV."). Although Goodrum et al. do not specifically disclose that the first plug-in unit addresses the second plug-in unit with the bus address, device-to-device transactions are well known in the art. An example of this is shown by Olarig from line 31 of column 9, "In the present invention, PCI device to PCI device transactions are also contemplated herein. When a PCI device on a physical PCI bus addresses another PCI device's memory or I/O addresses on the same physical PCI bus or on another physical PCI bus, this is referred to hereinafter as "peer-to-peer" PCI bus transactions. It is contemplated in the present invention that peer-to-peer transactions may be enabled or disabled by setting a control

register bit in the core logic. The present invention may broadcast the peer-to-peer transaction address onto the physical PCI buses so that the intended PCI target may respond. Once the target PCI device responds, the peer-to-peer transaction is completed. There is no host bus or memory bus activity required for peer-to-peer PCI bus transactions. Concurrent transaction activity may occur, however, on other physical PCI buses between the memory bus and/or host bus as more fully described hereinafter. This is especially useful when using intelligent, distributed input-output ("I/O") processing as more fully defined in the "Intelligent Input/Output" ("I.sub.2 O") specification, entitled "Intelligent I/O (I.sub.2 O) Architecture Specification," Draft Revision 1.5, dated March 1997; the disclosure of which is incorporated by reference hereinabove." A person of ordinary skill in the art at the time of the invention would have been motivated to perform a device-to-device transfer because there is a need to communicate between peer devices.

8. Claims 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6032271 to Goodrum et al. as applied to claims 1 and 4 above, and in further view of "CompactPCI Short Form Specification ". Referring to claims 3 and 5, although Goodrum et al. do not specifically disclose the first bus is a CompactPCI bus, CompactPCI is well known in the art as shown by the CompactPCI Short Form Specification. A person of ordinary skill in the art at the time of the invention would have been motivated to use a CompactPCI bus because, from the second paragraph in column 1 of page 1, "CompactPCI is an adaptation of the *Peripheral Component Interconnect (PCI) Specification* for

industrial and/or embedded application requiring a more robust mechanical form factor than desktop PCI."

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 6032271 to Goodrum et al. as applied to claim 6 above, and in further view of "CompactPCI Short Form Specification ". Referring to claim 8, although Goodrum et al. do not specifically disclose the first bus is a CompactPCI bus, CompactPCI is well known in the art as shown by the CompactPCI Short Form Specification. A person of ordinary skill in the art at the time of the invention would have been motivated to use a CompactPCI bus because, from the second paragraph in column 1 of page 1, "CompactPCI is an adaptation of the *Peripheral Component Interconnect (PCI) Specification* for industrial and/or embedded application requiring a more robust mechanical form factor than desktop PCI."

***Conclusion***

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US 4951283 to Mastrocola et al.

US 5815647 to Buckland et al.

US 5978938 to Kaiser et al.

US 6311296 to Congdon

US 6510532 to Pelly et al.

US 6523140 to Ardnt et al.

US 2001/0042225 to Cepulis et al.

US 2002/0124207 to Ohwada

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (703) 308-7298. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel, Jr. can be reached on (703) 305-9713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gc

SCOTT BADERMAN
PRIMARY EXAMINER